Camera electronics for the 72-channel S.A.O. Megacam

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ABSTRACT

The S.A.O. Megacam focal plane will consist of 36 large CCDs (2K X 4.5K format), each with 2 output ports running at pixel rates up to 200 kHz. The unbinned data field is thus as large as 324 megawords and is presented at a sustained data rate during readout approaching 28 megabytes/sec. We have developed a simple camera controller to deal with the problem of handling so many channels and their digitized outputs at fairly high speeds. We also present some results from ongoing efforts to optimize the 200 kHz signal processing chain for low noise and low crosstalk.

Keywords: camera, electronics, controller, CCD

The S.A.O. Megacam[1,2] represents an order-of-magnitude jump in the scale of the electronic controllers and signal processors that we have used in the recent past. In addition to that large number of video channels (72) to be accommodated, we desired to increase the readout rate to approximately 200 kHz in order to get the readout latency times down to comfortable levels, and to adapt the same controller hardware to allow autoguiding from two additional CCDs in the main focal plane. It soon became evident that adapting a commercial CCD controller to this vastly expanded task would be very problematic if not impossible. Thus, we were faced with the task of designing and building most of the camera in-house. Fortunately, based on our experience in past years with custom controller development, we were able to undertake this job with some prospect for success by basing the design on simple ROM/RAM modules for pattern generation, with which we had considerable favorable experience. We were quite confident that such a digital design, using proven techniques and incorporating the latest in digital components (such as gate arrays) would ultimately give us a very reliable, compact digital core for our controller. More challenging would be providing a high-speed fiber-optic link to the computer for the huge data stream and developing the higher speed analog signal processing chain we desired.

1. THE COMPUTER INTERFACE

It is often the case that the description of the computer link to a camera system is left to last. We choose to mention it first because the availability of a commercial solution was so crucial in our decision to proceed at all with this development program. We had experience in the past with some nonoptimal and unreliable computer interfaces in purchased systems, even when working at modest data rates, and were sensitive to the difficulties that would be experienced in moving to a much higher bandwidth regime. We also felt that we had neither the manpower nor time/money to try to engineer a custom solution ourselves.

The most attractive commercial system we initially found was from EDT Inc. Originally developed for fairly large digital camera systems such as the Kodak Megaplus CCD cameras, the interface consists of an SBus DMA interface with fiber-optic I/O link (the SCD-FOI) and a remote camera interface at the other end of the twin fiber link, the SDV module. I/O connection to the camera from the SDV is via differential digital links using standard RS422 differential drivers and receivers. Also provided is a fairly mature set of Solaris software drivers and formatting tools, which helped relieve our software team of many development tasks in setting up and using the interface.

Initially, we contemplated using two of these EDT interfaces in parallel into one Sun computer, as the bandwidth per interface became unreliable at about 24 Mbytes/sec, short of our goal of about 28 Mbytes/sec at full 200 kHz pixel rates. However, EDT has since developed a faster version which promises to provide up to 120 Mbytes/sec. This new version is based on the PCI bus, allowing it to be used in PC computers as well as the new Sun workstation products, which will also utilize this faster bus architecture. Thus, we now anticipate that our needs will be satisfied by a single interface link, sparing us both extra expense and complexity. We plan, however, to have a separate link (and indeed a separate computer) to handle the data stream from the two guide CCDs in the Megacam focal plane, since we want these to run asynchronously from the science imagers.

In testing the original SCD-FOI module for suitability for our task, we uncovered one feature that caused some initial problems. EDT had not anticipated that the output data stream from computer to camera might be more massive than a few control words. Thus, the interface initially came with just a 9600 baud serial link on the output side. Because we anticipated needing to transmit fairly large data fields to the camera in order to program such things as region-of-interest (ROI) subfield scanning (for autoguiding, for instance), such a slow output data rate from the computer was a problem. The hardware used for this link proved to have much higher bandwidth capabilities, however, and working with EDT engineers, we were able to raise this link to 115 kbaud at present and may ultimately approach 200 kbaud. To go faster would involve a major redesign of the interface board, but the present speeds are entirely sufficient for our applications, allowing a complete reprogramming of the camera in a fraction of a second.

2. THE DIGITAL CONTROLLER

We had previously developed a mixed ROM/RAM based controller for cameras with up to eight video channels, running at modest 50 kHz pixel rates. Since this concept had proven to be both robust and flexible enough for all the modes of operation we could envision for Megacam, we decided to base our new system on this type of hardware solution. Some experimentation was required to make sure that our most demanding application, autoguiding on a reduced ROI field, could also be accommodated, as we wished to use the same controller concept for this function as well (but separately packaged, and with its own interface). A prototype controller, using conventional TTL parts, has now been built and tested, a step we wanted to do before committing major effort and money into reducing the design to PC boards with VLSI logic devices.

It would have been possible to make the entire camera RAM-based, with all programming functions for all operational modes then downloaded from the computer. We chose instead to keep a portion of the fixed programs (e.g. full-frame imaging, with or without simple square binning) in ROM because of the advantages such a scheme offers for debugging and troubleshooting. When things occasionally go wrong, it is very important to be able to localize where the problem is, especially for nonspecialist field personnel. Having a camera which can be operated as a stand-alone element, with no computer interface at all, is a decided plus in such situations.

In Figures 1 and 2 we show a schematic overview of the Megacam controller system. Because the camera is so large physically and contains so many large CCDs, we have partitioned much of the driver and signal extraction functions into four modules around the circumference of the dewar, each servicing a quarter of the focal plane. The whole camera is controlled digitally, however, from a single module, which also interfaces to the EDT-supplied camera head communications link. A digital bus structure ties the four distributed modules together for sharing of the required timing signals. Individual boards in each module may be addressed for setting offset levels or querying an analog voltage setting. Data from the distributed 72 video channels is serialized locally and transmitted via differential lines to the camera head interface, where it is formed into the demultiplexed 16-bit wide data stream presented to the EDT camera interface module. This module in turn handles all the serial transmission protocols with the computer interface at the other end of the fiber link.

3. THE ANALOG SIGNAL CHAIN

Our desired pixel readout rate of 200 kHz represents about a factor of four increase over what we at SAO have routinely done in the past on low-noise CCD systems. It was very clear that none of our previously built analog chains had any hope of being adapted to this task. Settling times after both reset and charge transfer clock transients were in excess of 1 usec, which drastically cut into the available time for proper correlated double sampling (CDS) to be cleanly accomplished. Initial tests using familiar components from these systems showed unacceptable slowness at every stage of the chain, from the preamplifier right through to the buffer amps for the A/D converter at the end. Thus, we began a search for a new set of components, offering both good noise performance as well as much improved settling times for the more demanding task of processing our signals at this higher speed.

3.1 Preamplifier design.

It was clear that such old friends as the FET opamps AD745 or the OPA627/637 were not going to work well for this application. Although slew rates are good, settling times are very poor indeed for any precision. It also became clear that there was nothing newer and better in the way of low-noise FET opamps available from the manufacturers we surveyed. There were, however, several new low-noise bipolar opamps that seemed promising if coupled to an FET front end. Thus began a campaign to gather up samples of these new amplifiers from several manufacturers and to develop a series of test circuits to investigate their transient responses in a variety of simple configurations that could subsequently be miniaturized for mounting close to the CCD outputs inside the dewar.

The design we finally settled on is shown in Figure 3. It consists of an input dual FET (2N5564) operated in source-follower mode coupled to a high bandwidth opamp gain stage (AD829), with voltage divider feedback to the second FET input. This configuration, while not providing any front-end FET gain and thus relying on the opamp for this function, has the great advantage over an FET common-source input amplifier stage in having much better phase shift characteristics and is thus not nearly as prone to form an oscillator rather than a workable preamp. With very low noise opamps such as the AD829, this should not be a problem. Experimentation with several compensation schemes for this configuration showed that while shunt compensation and voltage feedback compensation were workable, the best performance was obtained with a simple current feedback compensation scheme, provided by a small capacitor from the inverting input to the compensation pin on the opamp. With this configuration, slew rates of 125 V/usec were obtained and settling times for a 10 volt step to about 0.1% were as low as 150 ns, with no tendencies to ring or exhibit long asymptotic tails.

3.2 The CDS signal chain.

Having now fashioned what we thought was a fairly fast preamp, we were unpleasantly surprised to find that the rest of the signal processing circuitry would prove to be equally challenging. The scheme we wished to implement was a fairly straightforward one, shown in detail in Figure 4. It consists of an input buffer stage, followed by a clamped capacitor restoration stage and dual-slope integrator for accomplishing the CDS function. The first problem arose with the clamped-capacitor buffer. Normally, we use an FET-input opamp for this element, but as in the case of the preamp, the quiet ones we have available are mostly too slow. The only very fast FET buffer we could find was the ancient LH0033, which suffers from a number of drawbacks. It is not specified for noise performance (or at least we could not find any), it eats a lot of power (over 20 ma quiescent), and is not available in modern miniature (SOIC) packaging for surface mounting. Provided that input bias currents are low enough, however, it now seems that a good bipolar input buffer may suffice for this application, and there are at least two good ones to choose from, the BUF04 from Analog Devices and the BUF634 from Burr-Brown. Both have under 4 nv/Hz$^{1/2}$ noise, input impedances in the 8-10 megohm range, low quiescent currents, and SOIC packaging is available. Experiments are under way to see if either exhibits a clear advantage for this application.

For most of the remaining amplifiers in the signal chain, with the exception of the integrator, which requires an FET input, we found that the LT1357/1358 series of low-noise bipolar opamps seemed to offer the best performance, preserving in large part the excellent transient response that we had strived for in the first stages. In particular, the dual LT1358 was especially attractive, as it is available in a small-format 8-contact SOIC, thus helping to make the PC board layout very compact.

We could find nothing better than the OPA627 for the integrator function. For this application the 627 has sufficient slew rate, and transient settling time is not an issue for an integrator of this sort. We also did some testing of various analog switches for clamping, resetting, and signal multiplexing for this part of the processing chain and came to the conclusion that the 201HS series from Harris or Analog Devices were both the fastest available and gave the lowest transients and offsets. Programmable offset for the final output from the analog electronics is provided by an AD7233 DAC 12-bit module.

For the last element in the chain, we are using the Datel ADS-937 fast 16-bit sampling A/D converter. Static and dynamic performance seems comparable to competing units, with a 1 usec acquisition + conversion time, differential nonlinearity of about 0.5 LSB, and no missing codes. We especially liked the small physical size and low power requirements for this device, allowing us to fairly easily achieve our goal of getting 4 complete analog channels on a 6U VME card along with all support electronics, both analog and digital.

Throughout the analog signal chain, we have sought to enhance channel separation using local voltage regulation wherever possible. Starting with each channel of preamplifier and continuing through the CDS circuitry to the A/D converter, we have used miniature 78LXX and 79LXX regulators to provide locally filtered +/-15V and +/-5V. Rated at about 100 ma over temperature and typically producing up to 150 ma, these are quite sufficient when used with the components we have chosen, giving us a compact yet effective way of shielding each channel from unwanted crosstalk.

4. ACKNOWLEDGEMENTS

The authors would like to thank Preben Noerregaard of Copenhagen University Observatory for many useful email discussions on preamplifier development.

5. REFERENCES

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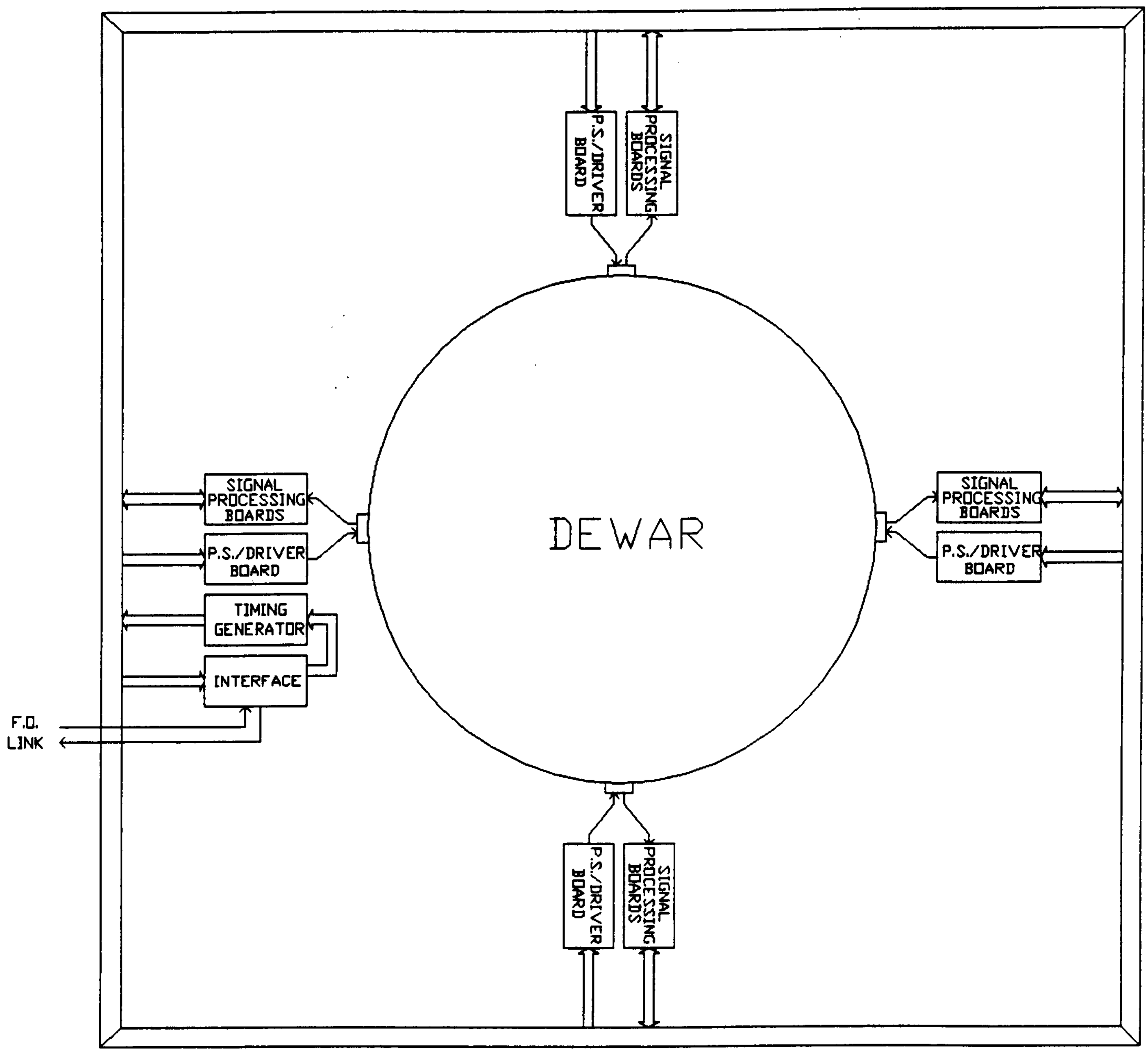

Figure 1. Physical partitioning of the S.A.O. Megacam. A single digital timing generator module transmits signals for CCD drive and signal processing to four ports around the circumference of the large dewar container, each handling up to nine 2K X 4.5K imagers (2 outputs each). Each signal processor board (four channels) will serialize its data and transmit to the camera interface, where the stream is demultiplexed and transmitted via fiber optic cable to the computer interface.

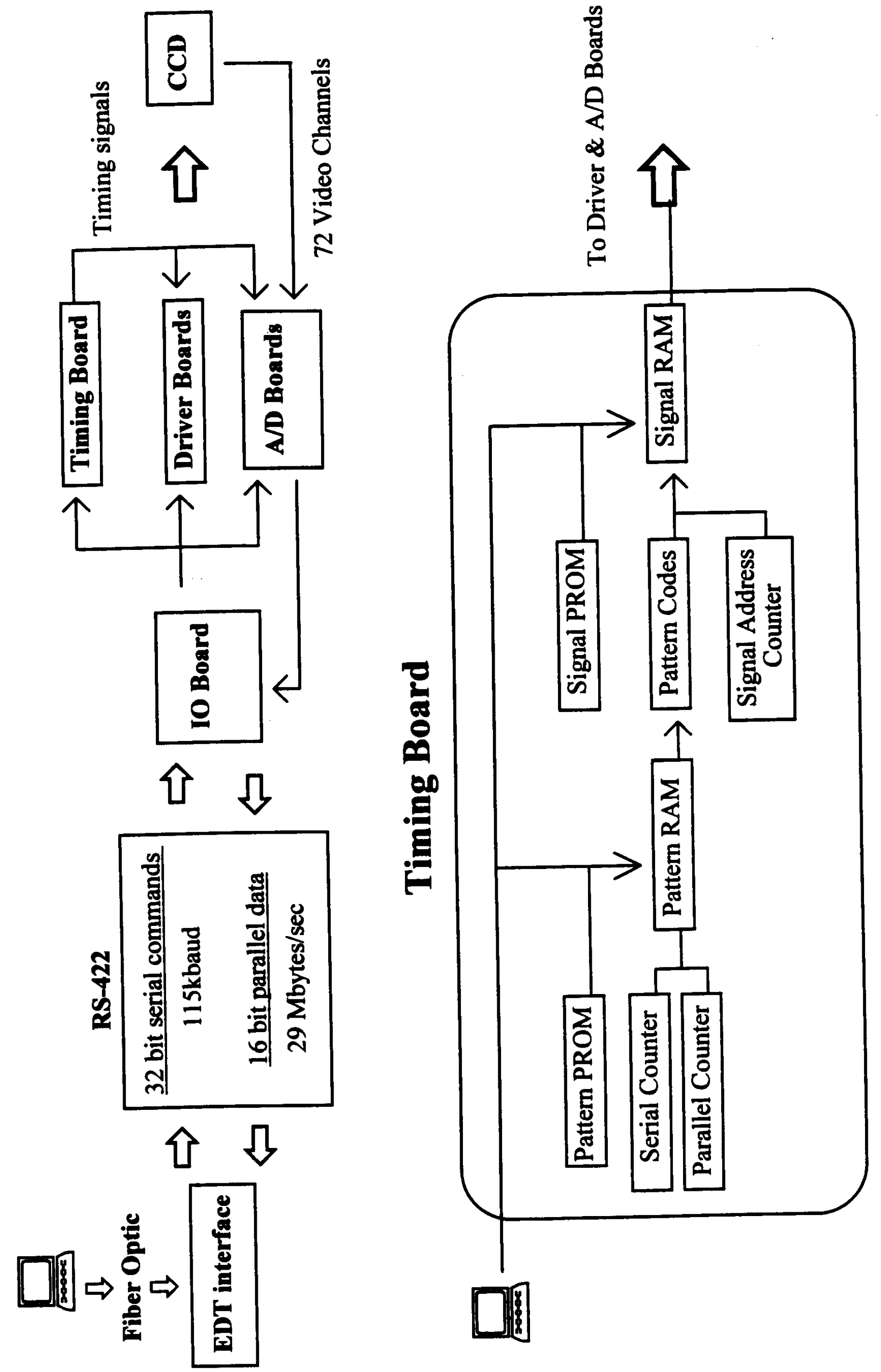

Figure 2. Block diagram for the timing generation and camera interface for the S.A.O. Megacam. Commonly used standard operating modes are stored in resident ROM, switchable with a single computer command. More detailed programming, such as might be needed for ROI framing for guiding, is available via a RAM sequencer, programmed from the host computer.

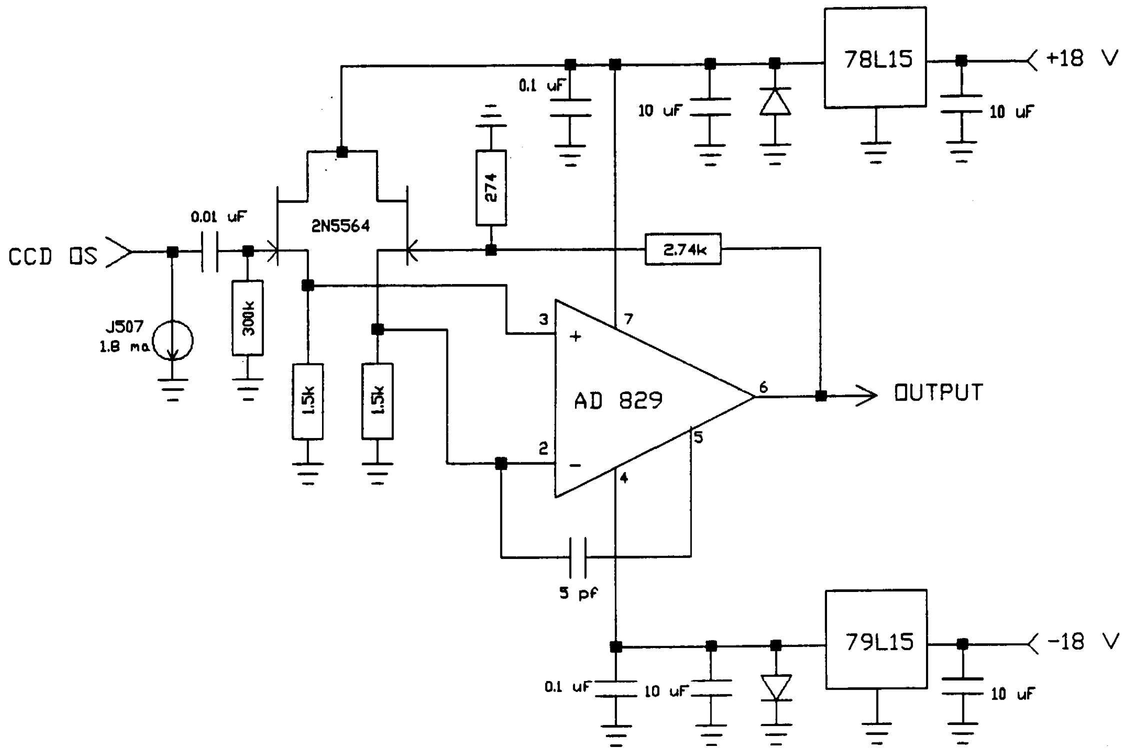

Figure 3. The fast-settling S.A.O. Megacam preamplifier design, utilizing the low-noise bipolar AD829 opamp with a 2N5564 dual JFET front end. Simple current feedback via the small 5 pf capacitor from inverting input to compensation pin proved effective in optimizing settling time.

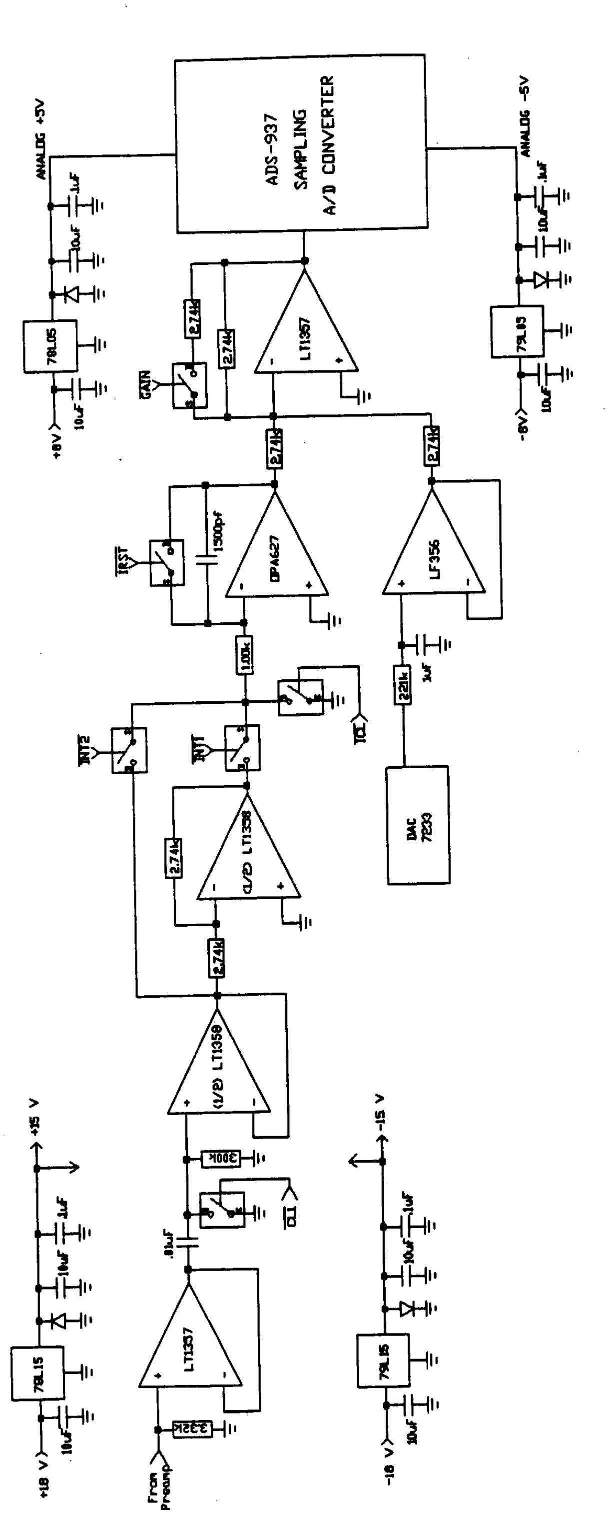

Figure 4. S.A.O. Megacam CDS signal processor, one of four channels per video processor board. Following baseline restoration on the clamped capacitor, inverted and noninverted signals are furnished to the analog integrator for CDS subtraction. Programmable offset and gain selection is provided to each channel.