Submillimeter Array Technical Memorandum

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Design Approach for the SMA Correlator

The SMA correlator is being built in a collobaration with a VLBI correlator. This approach is clearly reasonable because of the large degree of commonality in both instruments. The exploitation of similar architectures is a great advantage. However, the SMA project has some clear distinctions with the VLBI effort, We are constrained by a fixed budget and fixed delivery schedule that must remain tightly linked with the telescope construction. The penalty for a late conelator would be borne almost entirely by the SMA.

These differences also encompass divergent design philosophies for the correlator. The design for me VLBI correlators favors a very general and flexible design. The SMA prefers a very direct and simple solution, The division in philosophy is understandable considering the structures of the various projects.

A divergence in correlator design at some level is already an accepted fact. We feel the optimum separation in designs must consider both the maximum utilization of commonality and the widely differing goals of the projects. To this end, SMA is quite happy to accept some reduction in commonality and generality in order to meet the minimum requirements of our correlator in a timely and cost effective manner. Naturally, we expect the cot-relator to meet our specifications. We will (and have in the past) accepted sub-optimum decisions to promote commonality, but only in so far as it helps to expedite the design process.

Therefore, the following list of design issues should be considered. Any feature which exceeds these expectations is useful to the SMA, only if it furthers our goals for cost and delivery time. Thus we offer the following list to help define this philosophy.

1) Modes - Only the modes described in SMA technical memo #66 are necessary. This requirement can be met with commercially available parts, The proposed utilization of a custom part is a concern because it could create unnecessary delay.

2) Timing - The correlator data will be integrated by the DSP every10 msec. There will be a dead period of between 1 and 10 μsec between data switches. The timing will be controlled by hard-wired signals provided by SAO. The nature of these signals may be optimized for the convenience of the board designer. The DSP must be able to unload and process the data as per SMA technical Memo #65, which indicates a board unload period of 10 sec.

3) Test Patterns - The SAO station unit will generate test patterns to test the correlators and data paths. This internal test, in conjunction with an external board tester (off-line) is sufficient to test the correlator after delivery. An on-board test generator is unnecessary. It adds complexity and could compromise board speed.

4) Visibility - It is our position that the DSP should have complete control over the working of the correlator board. The DSP should be optimized for data processing throughput. The VME should access the DSP for data transfer, message passing and to load the code for the DSP chip. Additional interconnection is, (once again) a source of complexity and has the potential to delay our project..

5) Clock Speed - We are promoting a correlator clock speed of 53 Mhz, because it could produce a substantial cost savings for very little extra engineering effort. By using the SAO proposed switchs, the only limiting factor is the correlator chip itself, which is specified for 64 Mhz. We can accept a work-around if unforeseen problems are encountered *(i.e.* operate at a lower speed). We understand that this situation has some risk factor. However, in this case, the risk serves to further our goals.

It's hoped these points will help illustrate the differences in design philosophy between the SMA and VLBI correlators. We accept the desire for commonality and compromise, however, on the questions of delivery time and cost, compromise for unneeded complexity is not acceptable.