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Design and Performance of a Digital PLL for Gunn Oscillators

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The digital phaselock loop (PLL) described in this memo has been in use on the SubMillimeter Array (SMA) antennas on Mauna Kea for several months and was a key element in obtaining the first three-baseline phase closure on September 26, 2000. This unit is also being used by the Princeton MAT CMB[1] project, the Caltech Submillimeter Observatory[2] and in the initial tests of the ALMA antennas in Socorro by the NRAO/Tucson receiver group[3]. The design, performance and calibration steps are briefly described.

1 Introduction: Gunn oscillator frequency tuning

The output frequency ν of a cavity-tuned Gunn oscillator depends simultaneously on both the electrical and mechanical tuning. Specifically, ν is a function of the bias voltage V and the cavity length L:

$$\nu = f(V, L). \tag{1}$$

At a specified tuning point i, the function f can be approximated by a linear dependence in each variable independently, leading to the following differential equation:

$$\nu = \nu_i + \kappa_{V,i}\Delta V_i + \kappa_{L,i}\Delta L_i, \quad \text{where } \left.\frac{d\nu}{dV}\right|_i = \kappa_{V,i} \text{ and } \left.\frac{d\nu}{dL}\right|_i = \kappa_{L,i}\ . \tag{2}$$

Typically, $\kappa_{V,i}$ is listed in units of MHz volt^{-1} and is positive-valued, while $\kappa_{L,i}$ can be interpolated from a micrometer tuning curve listed in units of mil GHz^{-1} and is negative-valued. With the application of a phase lock loop, ν can be held constant in time at ν_i as it can actively shift the bias voltage by $\Delta V(t)$ in order to offset temporal changes in the cavity length $\Delta L(t)$. Much of ΔL is due to drifts in the room temperature. Thus, a successful PLL must be able to maintain lock through a sufficient range of tuning voltage to counteract temperature fluctuations.

2 Design of a Digital PLL

To promote the benefits of modularity and reduce the number of cables emerging from the optics cage, we decided to provide a PLL for each LO assembly. This requirement set constraints on the size of the unit. Three separate sections comprise the PLL package shown in Figure 1. The righthand side of the PLL box contains a microwave diplexer which allows the high-frequency signal (6-8 GHz) to pass from the YIG reference input out to the harmonic mixer. At the same time, it allows the low frequency mixing product (0-1 GHz) to return from the harmonic mixer and to enter the two-stage IF amplifier.

2.1 Diplexer and IF Amplifier

The diplexer substrate is manufactured from Arlon AR1000 Ceramic powder-filled, woven fiberglass, PTFE composite with a dielectric constant of 10. The IF amplifier is comprised of two stages of amplification via Hewlett-Packard INA-02184 Low Noise, Cascadable Silicon Bipolar MMIC Amplifiers for a total gain of $\approx$ 65 dB. This large gain is necessary to process the tiny signal returning from the harmonic mixer (which itself views the Gunn signal through a 20 dB tap). With such a large gain, suppression of noise at the amplifier input port is crucial to prevent oscillation. The tight-fitting lid provides a good mechanical enclosure that prevents any noise coupling. Also, to minimize temperature changes in the unit at power-up time (and the accompanying phase drifts), a heater resistor is installed in the block which can be enabled by the microcontroller when the PLL/LO chain is turned off.

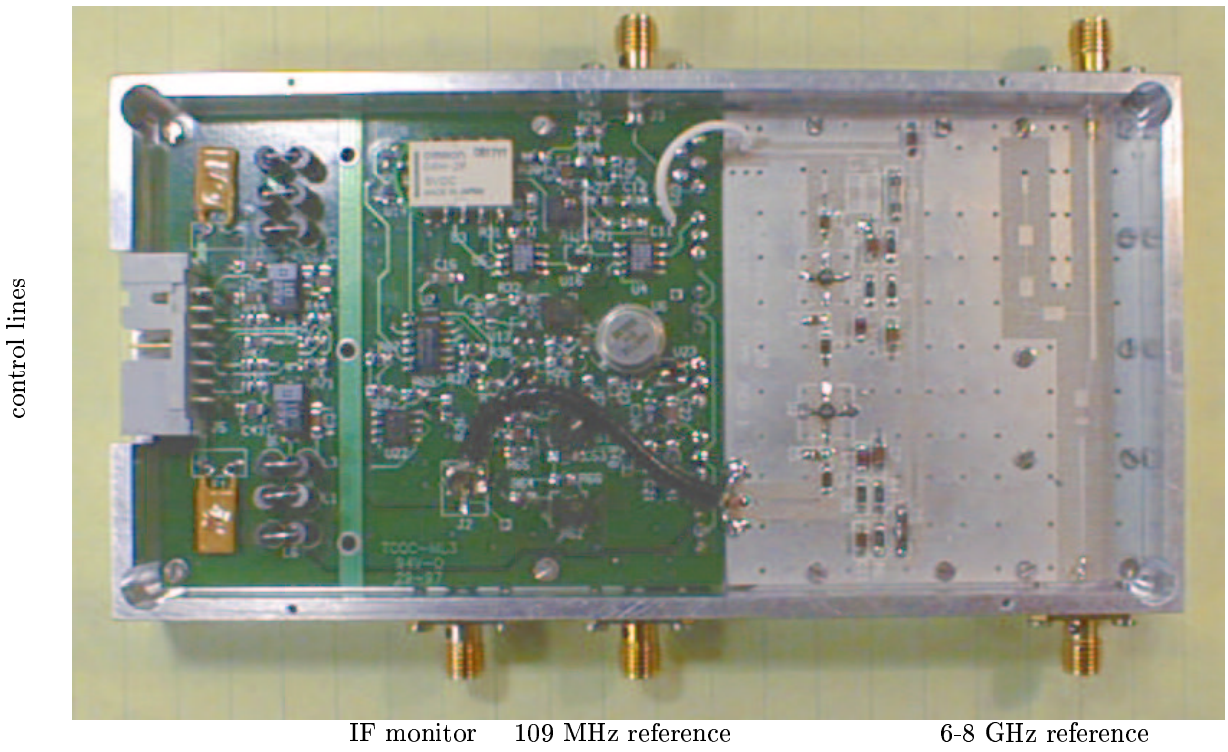


Figure 1: Top view of the digital PLL with the lid removed.

2.2 Phaselock electronics

A good description of PLLs is given by Gardner (1979). Our PLL is based on a high-gain second-order loop with an active filter and a microcontroller interface. A schematic drawing of the circuit can be found on the web[4]. After amplification, the IF signal is passed to the Analog Devices AD96687 Ultrafast ECL Dual Comparator which converts the sinewave to a squarewave. We use zero crossing detection in the comparator in order to avoid an automatic gain control (AGC) circuit in the IF amplifier. Also, by biasing the comparator above the peak value of the IF signal, the microcontroller can disable the loop. The digitized signal output from the comparator enters the Analog Devices AD9901 Ultrahigh Speed Phase/Frequency Discriminator. Here we implement a loop gain control by controlling the current in the AD9901. Specifically, the loop gain of this system (along with the loop bandwidth) is determined by a damping resistor (the parallel combination of potentiometer R19 and resistor R75) and an integrating capacitor (C9). The choice of these values depends on the noise characteristics of the oscillator and the loop performance specifications. For the SMA, the design specification requires the PLL to reacquire lock within $t = 2\mu$s of a Walsh function phase change. The relationships between the rise time (t_r) and the 1% settling time of a servo loop (t_s) and its undamped natural frequency (ω_n) are given by:

$$t_r = \frac{1.8}{\omega_n} \tag{3}$$

$$t_s = \frac{4.6}{\sigma} = \frac{4.6}{\zeta\omega_n} \tag{4}$$

where ζ is the damping factor and σ is the negative real part of the pole (Franklin, Powell & Emami-Naeini, 1994). With a reasonable choice of damping factor $\zeta = 0.707$, we require $\omega_n = 2\pi \times (0.6$ MHz), which

corresponds to:

$$\omega_n = \sqrt{\frac{K_o K_d}{R_1 C}} = 2\pi \times (0.6\text{E}+06) \text{ radian second}^{-1}. \quad (5)$$

where K_o is the gain of the tunable oscillator in radian second^{-1} Volt^{-1}, and K_d is the gain of the phase detector in Volt radian^{-1}. For Carlstrom Gunns, K_o is on the order of 300 MHz V^{-1} = 2.0E+09 rad s^{-1} V^{-1}. For our phase detector (AD9901), the maximum value of K_d is 0.285 Volt radian^{-1}. However, for tuning flexibility, we need to operate at a gain in the middle of this range, so we choose 0.15 V rad^{-1}. With this information in hand, we compute the product (R_1C) must be 2.0E−05. In the circuit, we use R_1 = 1kΩ to convert the square wave into a DC voltage. This means that C must be 20 nF. Finally, we can relate all of these variables back to the damping factor:

$$\zeta = \frac{\tau_2 \omega_n}{2} = \frac{R_2 C \omega_n}{2} = 0.707. \quad (6)$$

With this condition, we can solve for the final variable, R_2:

$$R_2 = \frac{1.414}{C\omega_n} = 18\Omega. \quad (7)$$

An AD817 High Speed, Low Power Wide Supply Range Amplifier provides the loop integrator. A second AD817 monitors the Gunn bias voltage and, along with the Fairchild BAV99LT1 ultrafast diode pair, keeps it within ±0.6 V (a diode potential) of the target bias voltage set manually via potentiometer R33. The locking sideband can be selected digitally via an Omron G6H-2F DC5 Low Signal Relay. An IF monitor port of −20 dB is provided for viewing the phaselock quality on a spectrum analyzer.

2.3 Lock detection

By the nature of the design, phase lock is indicated whenever the gunn bias voltage lies between the two voltage limits established by the diode pair. However, if the IF amplifier is being overdriven, it is possible to "lock" on a harmonic of the IF. To reject these false "locks", two LC circuits are included which provide a simple yet powerful analysis of the IF to the tuning software. A portion of the IF signal is tapped and sent through a notch filter tuned to 109 MHz and on to an Agilent HSMS2812 Schottky Diode pair. A similar circuit implements a bandpass filter tuned to the same frequency. The voltage outputs of both filter circuits are digitized by the microcontroller board and used in the automated phaselock algorithm.

3 Performance

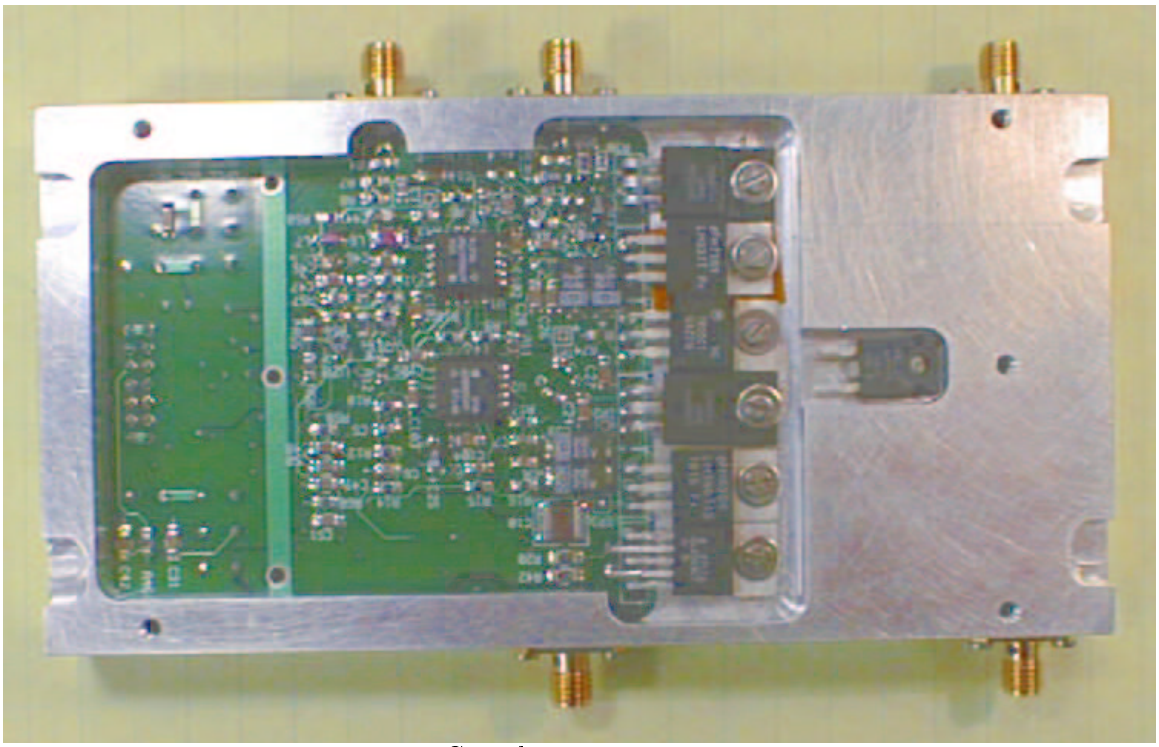
3.1 Adjacent channel power

The quality of phase lock can be assessed by the amount of power outside of a delta function at the IF frequency compared to the power within the delta function. We refer to this ratio as the adjacent channel power and obtain values of −35 to −40 dBc on Carlstrom Gunns using Pacific Millimeter[5] FMA harmonic mixers (even harmonics only). A representative plot from a spectrum analzyer is shown in Figure 3.

3.2 Walsh functions

The PLL easily maintains phase lock throughout the application of phase-switching Walsh functions imposed on the low-frequency 109 MHz reference from the SMA direct digital synthesizer. It has been lab-tested with a Walsh-function emulator which introduces a 90° phase change at 100 Hz. At the proper gain setting, it reacquires lock well within the design specification (Figure 4) and has sufficient gain adjustability to compensate for the variation in the inherent oscillator gain across the receiver band.

IF monitor 109 MHz reference 6-8 GHz reference



Gunn bias output Harmonic mixer

Figure 2: Bottom view of the digital PLL.

3.3 Locking range

The ±0.6 volt locking range provided by the PLL allows it to maintain lock during substantial drifts of ambient temperature. To quantify the PLL performance, we have measured the tuning characteristics for the two types of Gunn oscillators and present the results in Table 1.

The main quantity of interest is the amount of temperature drift (ΔT) the PLL can accommodate before losing lock. For the Gunns tested here at this particular frequency, the corresponding values are:

$$\text{H188} : \Delta T = (0.6\text{V})(150\text{MHz V}^{-1})(27.5\text{MHz } (^\circ\text{C})^{-1})^{-1} = 3.3^\circ\text{C} \quad (8)$$

$$\text{H263} : \Delta T = (0.6\text{V})(330\text{MHz V}^{-1})(9.8\text{MHz } (^\circ\text{C})^{-1})^{-1} = 20.2^\circ\text{C} \quad (9)$$

Clearly the Gunns with brass tuning shafts (i.e. same material as body) are preferred for the best phase lock performance and overall system stability. Active control of the ambient temperature in the antenna receiver cabin is also important.

Table 1

Gunn Serial Number	tuning shaft material	ν (GHz)	κ_V mil GHz^{-1}	κ_L^{-1} MHz Volt^{-1}	temperature coefficient MHz ($^\circ$ C)$^{-1}$
H188	stainless steel	115.0	1.15	150	27.5
H263	brass	115.0	1.05	330	9.8

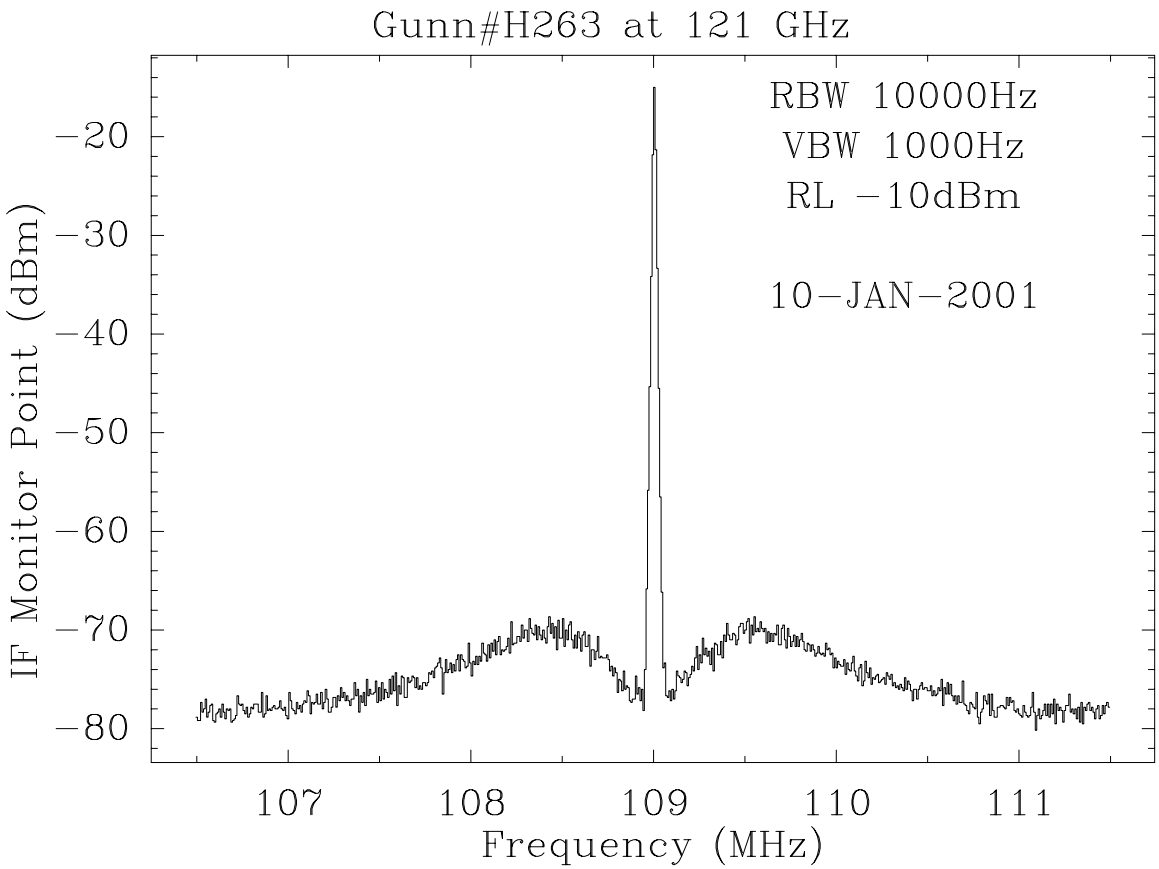


Figure 3: Typical IF monitor signal from a Gunn oscillator phaselocked at 121 GHz.

4 Calibration of a new unit before usage

For each new digital phase lock loop circuit that is contructed, the following steps must be completed before it can be used on the telescope:

- Place serial number label and labels on the five SMA ports
- Set the nominal Gunn bias potentiometer
- Set the notch filter offset potentiometer
- Set the bandpass filter offset potentiometer
- Adjust the RC circuit to 109 MHz on the notch filter
- Adjust the RC circuit to 109 MHz on the bandpass filter
- Set the Gunn active loop damping potentiometer
- Put copper tape on the lid walls
- Run the tune6 command "testamp" to view the bandpass
- Confirm the microcontroller ADC value for the Gunn bias
- Measure the lock sensitivity to reference power
- Verify a clean lock trace on the spectrum analyzer
- Measure the 109MHz leakage
- Install the heater resistor

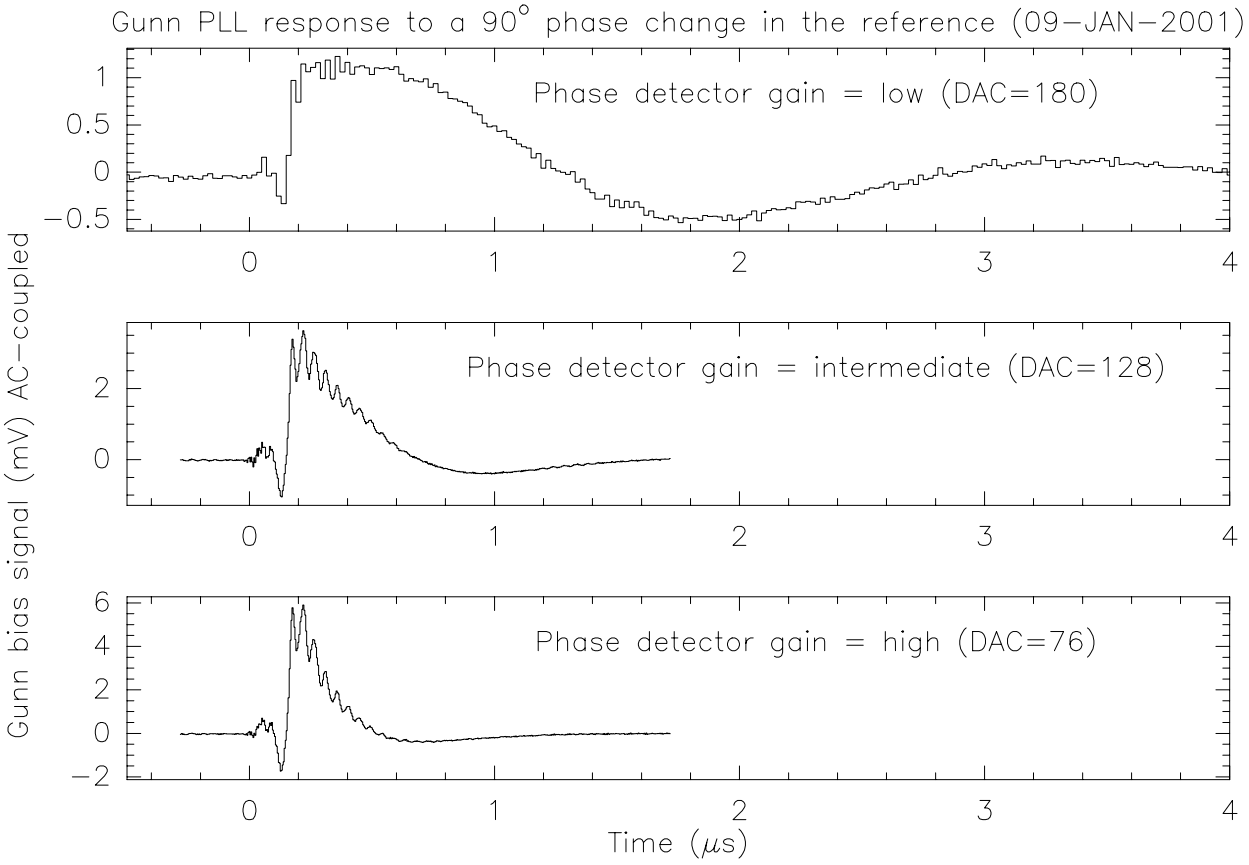


Figure 4: Example of the fast relocking capability of the PLL for various programmable loop gain settings. DAC=0 corresponds to 0 Volts and represents maximum gain (quickest response). DAC=255 corresponds to 5 Volts and represents minimum gain (slowest response).

4.1 Attach labels

Each PLL is assigned a serial number label in the format "dpllxx" where "xx" is a decimal number with a leading zero, if necessary. Also, the following labels should be placed on the top plate: "IF MON", "109 REF", "YIG REF", "HARM MXR" and "GUNN BIAS".

4.2 Mechanical mounting

Be sure that the diplexer board and the digital board are securely screwed into the box.

4.3 Gunn bias pot

The Gunn bias pot is R33 on the PLL board. U7 is the LM324 14-pin DIP. Pin 7 of U_7 is OUT2 which is the point to monitor. Measure this voltage with respect to the chassis ground. Adjust the pot to bring it to the nominal voltage (e.g. 8.6 V). You must turn on the Gunn before doing this, of course. You may either use the "b1testgunn" EPROM, or use the regular "b1t4.hex" EPROM and issue the "gunn on" command in tune6 (or using the Palm pilot program "busmaster"). Now measure the Gunn bias voltage emerging from the SMA connector. It should be at one of the rails (8.6±0.6 V). IF it is only 8.6±0.3 V, then you have probably installed the resistors R36 (5kΩ) and R37 (33.2kΩ) incorrectly. Their four pads form a square.

They should be placed horizontally on these pads, and not vertically. If instead, the voltage is 12 or 13V, then check the U16 diode. It should be an anti-parallel diode, not just a single diode. Also, check that the R75 resistor value is correct (two 51.1Ω resistors soldered on top of each other).

4.4 Notch filter offset

The notch filter offset pot is R62 on the PLL board. Put an SMA grounding cap on the harmonic mixer input port. Use the "v" command in tune6, or use the Palm pilot to monitor the notch filter value and adjust the pot until the value is zero or just above zero. For reference, a single A/D bit is approximately 5 mV. If you are unable to set the offset to zero, then the first-stage IF amplifier may be oscillating. Make sure you have flattened the legs before soldering it onto the board.

4.5 Bandpass filter offset

The bandpass filter offset pot is R61 on the PLL board. Follow the same instructions as for the Notch filter offset.

4.6 Notch filter center frequency

The nominal values for the filter are C44=4.5pF, L8=470nH and R59=10kΩ. Connect a GPIB-ready synthesizer to the harmonic mixer input. Run the tune6 command "calibrate filters" to calibrate the filters. Take the resulting data file (if_filters.response) and run it through the GRAPHIC macro combinefilters.graphic to plot the results (see Figure 5). Adjust the filter component values to bring the centers of each filter to 109 ± 1 MHz. Note that a capacitance change of 0.1 pF moves the frequency by roughly 1 MHz.

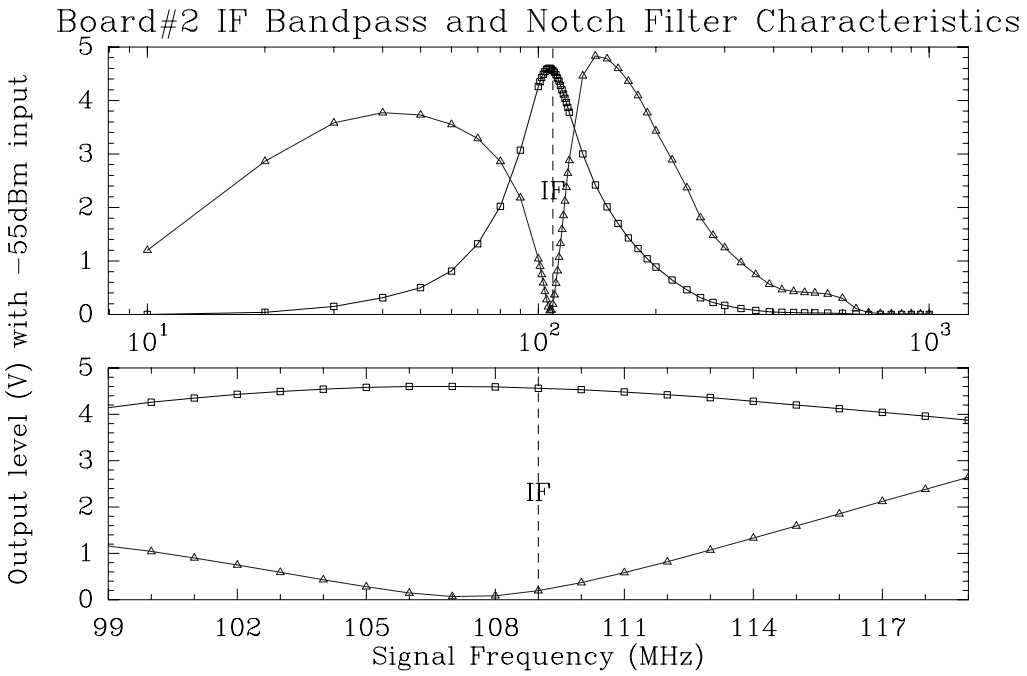


Figure 5: Plot of the data file generated by the tune6 command "calibrate filters". The IF bandpass and notch filter responses are shown.

4.7 Bandpass filter center frequency

The nominal values for the filter are C45=21pF, L7=100nH and R60=10kΩ. Follow the same instructions as for the Notch filter.

4.8 PLL active loop damping pot

The resistor R_2 is implemented by the damping pot on the PLL board which is R19 on the silkscreen. Measure the resistance between the center pin and the pin above the "1" in "R19" (or, effectively, pin 2 of U4). Set the pot such that the resistance equals the nominal value calculated in section 2.2. Try to lock a Gunn. Once it is locked, use the tune6 "gain" command to set different values of the gain (i.e. 80, 128, 160, 200). You should see the shoulders of the trace change position and strength. If you see no change, then you may have a problem on the PLL board. Check to see that R27 is not shorted out (by a solder bridge) to the adjacent via hole.

4.9 Copper tape on the lid

To provide maximum isolation of the chamber containing the IF amplifier, place strips of copper tape on two of the three barriers that hang down from the box lid. The two you want are the two closest to each other. On the end barrier, a single piece of 1 inch wide tape should fold and go all the way down the barrier on both sides. On the middle barrier, the tape should approach no closer than 0.3 inches from the Gunn bias edge of the box, and no closer than 0.6 inches from the YIG reference edge of the box. This is to avoid shorting out the IF traces. In general, use two layers of tape on each barrier. But be sure that the lid does not rock. You might need to use 3 layers on the end barrier to prevent this. Also, you should scrunch a bit of copper tape into the small voids between the diplexer void and the aluminum wall. The bit should go under the area where the wall touches the diplexer, so as to fully seal the chamber.

4.10 Plot the amplifier bandpass to check the gain and look for oscillations

Assemble a spectrum analyzer and a synthesizer onto the GPIB bus. Connect the spectrum analyzer to the IF monitor point of the PLL box. With the RF power OFF, connect the synthesizer output to the harmonic mixer input point on the PLL box. Run the tune6 command "testamp -s [pllSerialNumber]" to view and record the bandpass of the IF amplifiers. This command will inject −60dBm signal at 109 MHz and record a trace into the file testamp_dpllxx.trace, and display it on the screen using wish and a tcl script. If the amplifiers are working properly, you should see about −20dBm at the monitor point (at 1MHz resolution bandwidth on the spectrum analyzer). Now set the frequency to 800MHz. You should see the signal reduced to about −55dBm at the monitor point.

Now, disconnect everything from the harmonic mixer port. The response curve should remain smooth with no oscillations (see Figure 6). If instead you see a strong signal (anything above −50 dBM) at 700 or 800 MHz, it is an IF amplifier oscillation that should be fixed. To fix it, first remove the PLL box lid and verify that bandwidth control capacitor (C4) is a porcelain 33pF device (made by ATC). Second, verify that inductor L2 is 220nH. Finally, examine the solder joints of the two IF amplifiers. Solder should be placed on all the legs as close as possible to the device. This should kill the oscillation. If not, then revisit the section on copper tape (section 4.9), with particular attention to the voids between the diplexer board and the wall of the box.

If you do not want to open the PLL box to fix it, a stop-gap measure is to place a 1dB pad on the output to the harmonic mixer. This will also kill the oscillation. Even if you do nothing, once the ∼10dBm synthesizer (or YIG) signal is applied, the oscillation always disappears (since the impedance of the harmonic mixer changes).

4.11 Confirm the microcontroller ADC value for the Gunn bias

Place the Gunn bias output on a multimeter. Run "v" in tune6 (or "b1testADCs" on the Palm) and look at the digitized Gunn bias value. The two values should be within 5-10 mV. If they are not, first check that the voltage-dividing resistor network has the correct values (20kΩ for R34 and 10kΩ for R35), and that

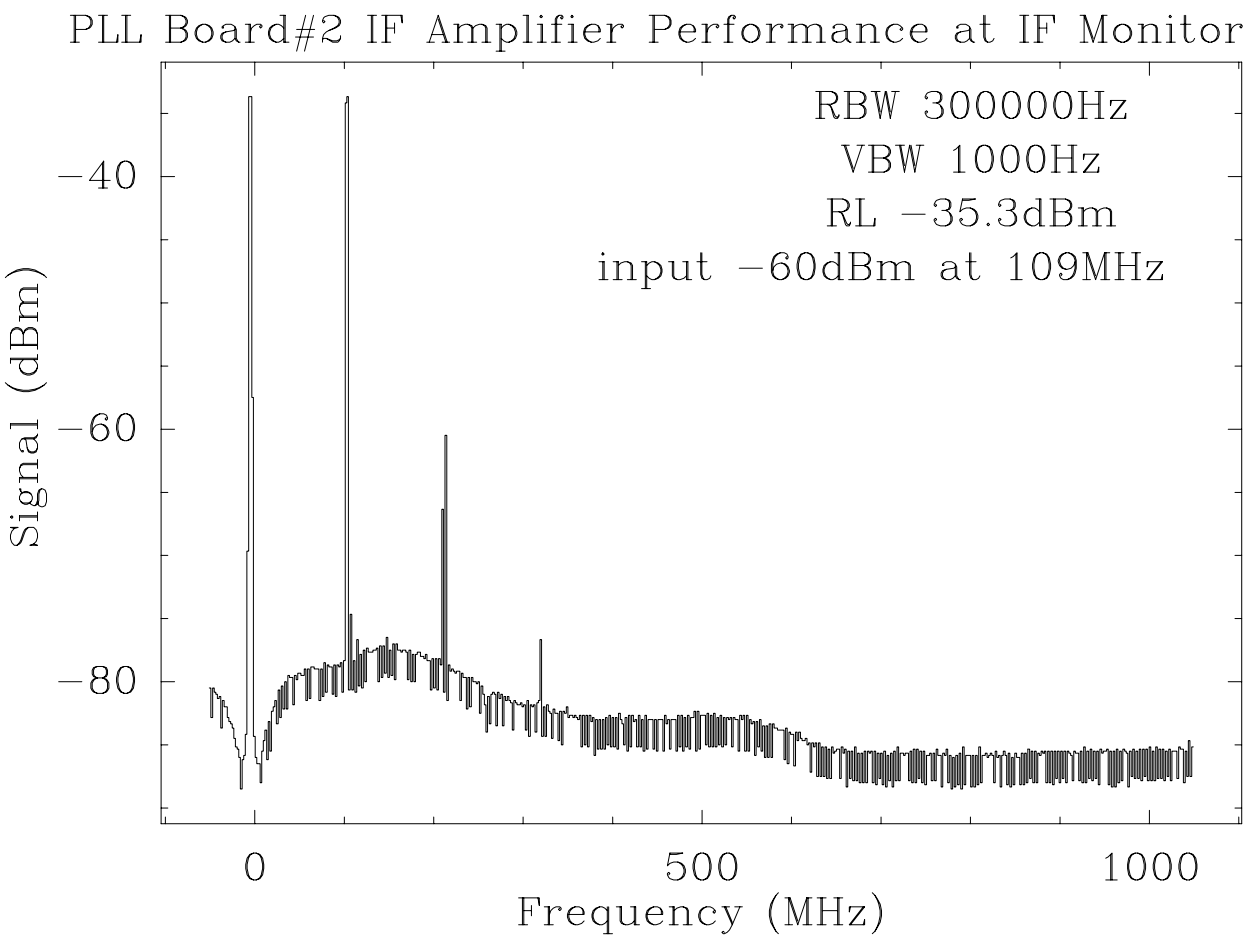


Figure 6: Plot of the data file generated by the tune6 command "testamp". The IF amplifier bandpass is shown along with the test tone (and its harmonics).

the other ADC inputs are not saturated. If the resistor values are correct, then you should add trimming resistors on top of the original resistors to bring the digitized voltage into better agreement with the actual voltage. Use the following formulas:

$$Q = \frac{V_{ADC}}{V_{true}} \tag{10}$$

$$\text{if } V_{ADC} > V_{true}, \text{then add to R35}: \; R = \frac{20000}{3(Q-1)} \tag{11}$$

$$\text{if } V_{ADC} < V_{true}, \text{then add to R34}: \; R = \frac{20000}{3}\frac{(3Q-2)}{(1-Q)} \tag{12}$$

4.12 Measure the lock sensitivity to reference power

First lock the Gunn to some frequency. Then turn down the 109 MHz reference signal power to -30 dBM and see if phase lock is maintained. This can be accomplished by installing a 20 dB and a 10 dB attenuator in line with the Fluke 6160B synthesizer set to its lowest output power setting. A PLL in good shape will be retain lock. Next, disable both references, the Gunn itself and the PLL for a time, then re-enable then. The PLL should re-acquire lock even at this low reference level. The power level where lock is lost appears to be -35 dBM, while lock is regained at -33 dBM.

4.13 Verify a clean lock trace on the spectrum analyzer

The lock signal should look like Figure 3, with symmetric shoulders surrounding the delta function. If there are sidebands around 860 kHz and 1700 kHz, then check to see if the bypass capacitors (e.g. C30) around the negative regulators are present. Without these, the regulators can oscillate and produce artifacts in the lock loop. In a wider frequency span display, you might also see faint lines at 0.5 and 1.5 times the IF frequency. We believe these are due to the fundamental frequency of the Gunn (0.5 times its primary output frequency) propagating to the harmonic mixer and mixing with half the harmonic of the YIG reference compared to the main Gunn signal. The evidence for this is that the lines disappear if you tune the YIG to an odd harmonic (since the fundamental cannot mix with a non-integer harmonic). In any case, these lines should not be anything to worry about.

4.14 Measure the 109MHz leakage

Some of the 109MHz reference power entering the PLL box can leak back into the IF amplifier and mimic the signal returned from the harmonic mixer. At low levels (< -40dBM as seen on the IF monitor port) this leakage is not a problem. However, larger values (e.g. -33dBM) can prevent the PLL from locking as it rivals the power of the Gunn signal. Connect a 109MHz signal of $+13$dBM (this is the maximum that the Fluke 6160B synthesizer can deliver) into the 109MHz reference port on the PLL and look at the IF monitor signal on the spectrum analyzer. If the value is above -40dBM, try putting down more copper tape (as in section 4.9) to reduce the level.

4.15 Install the heater resistor

One side of the 50Ω heater resistor should be connected to the test point TP1 (which goes to the collector = pin 3 of U23). The other side of the resistor should be connected to ground (we solder it to pin 1 of the U11 regulator). The emitter of U23 is connected to +5V, thus when the heater is enabled, there should be only 100mA drawn. The collector pin is labelled "FETBIAS" on the schematic. If you see 18V across the resistor, then somehow you have wired it incorrectly.

4.16 What if it doesn't lock?

If everything is set right and the PLL refuses to lock, you should first check the quality of the soldering on the SMA connectors under a microscope. The solder joint on the SMA connector pin carrying the 109MHz reference may need to be reheated. If the connections are okay, then check out the phase-frequency detector. Put an RF signal (30-150MHz) on the reference and signal inputs (with some phase shift between them). You can do this by connecting a synthesizer output to the 109MHz reference input port on the PLL, and through 60dB of attenuation to the harmonic mixer port. Look at the output of the comparator (U1) on an oscilloscope. You should see an RF signal. Then compare the input and output pins of the AD9901 phase-frequency discriminator (U2). If you don't see any output, try changing the chip. You should see the phase of the two waveforms change as you lower the frequency of the signal. Be sure to blink the PLL everytime you change frequency or else the chip may go into never-never land and you won't see a signal. If after blinking it, you still don't see the proper output, you may have to replace the AD9901.

4.17 What if it oscillates at 700 or 800 MHz?

See section 4.10.

5 References

[1]http://imogen.princeton.edu/mat/instrument/

[2]http://www.submm.caltech.edu/cso/

[3]http://www.tuc.nrao.edu/almatuc/

[4]http://cfa-www.harvard.edu/~thunter/schematics/digitalPLL.ps

[5]http://pacificmillimeter.com/

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