Antenna IF Simulator Assembly

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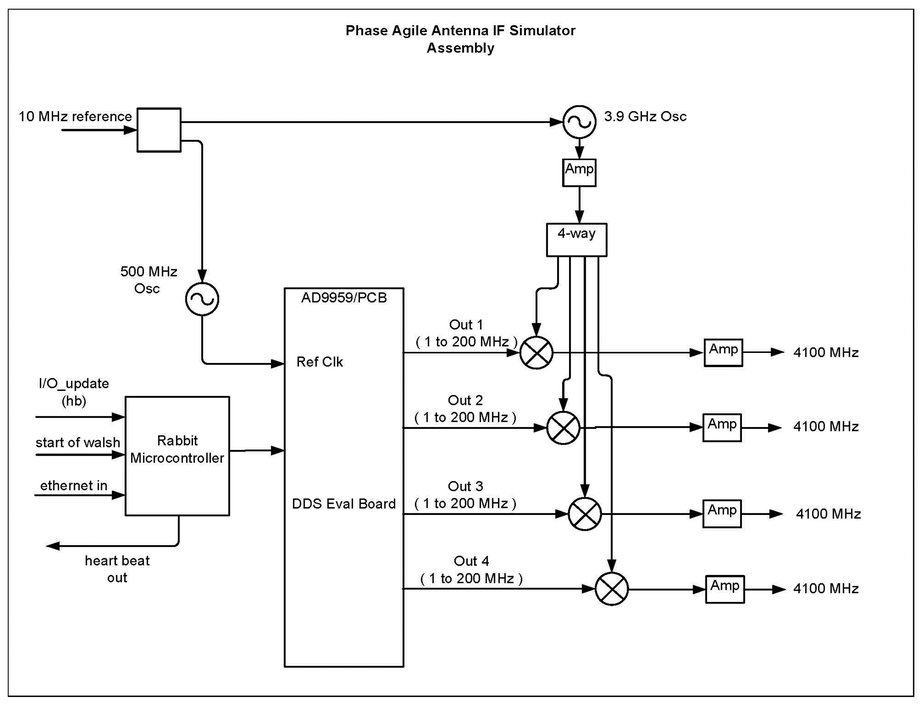
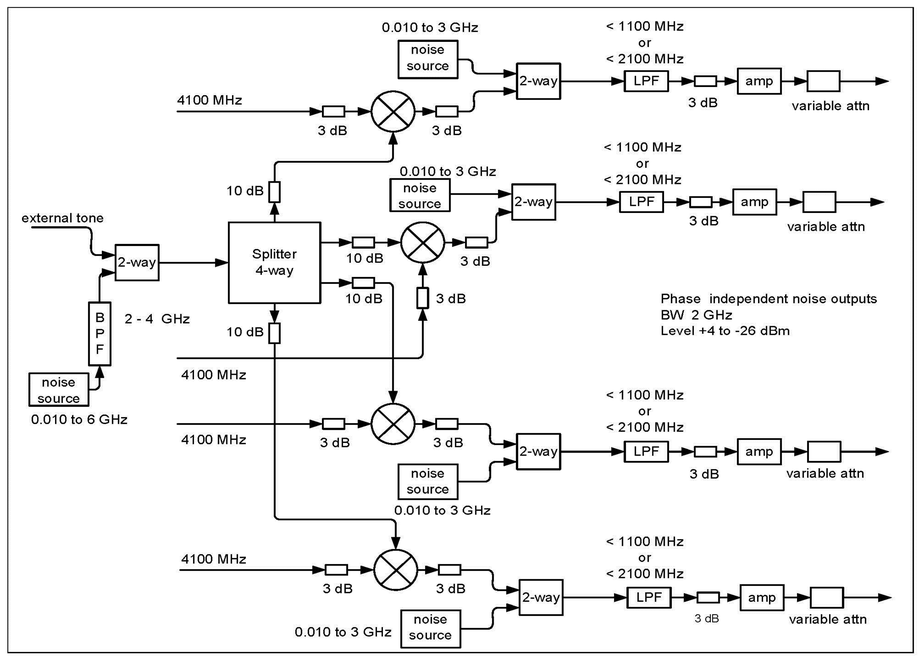
Introduction

Objective: Design an IF system for use in the development of FPGA bit code for the new digital back end (SWARM) in the SMA Cambridge laboratory. The system should function as closely to the analog back end of the SMA array as possible. It will generate 4 blocks of phase programmable 2 GHz wide noise to be used as inputs for ADCs located in the ROACH2 assemblies. The antenna IF simulator system will provide the following:

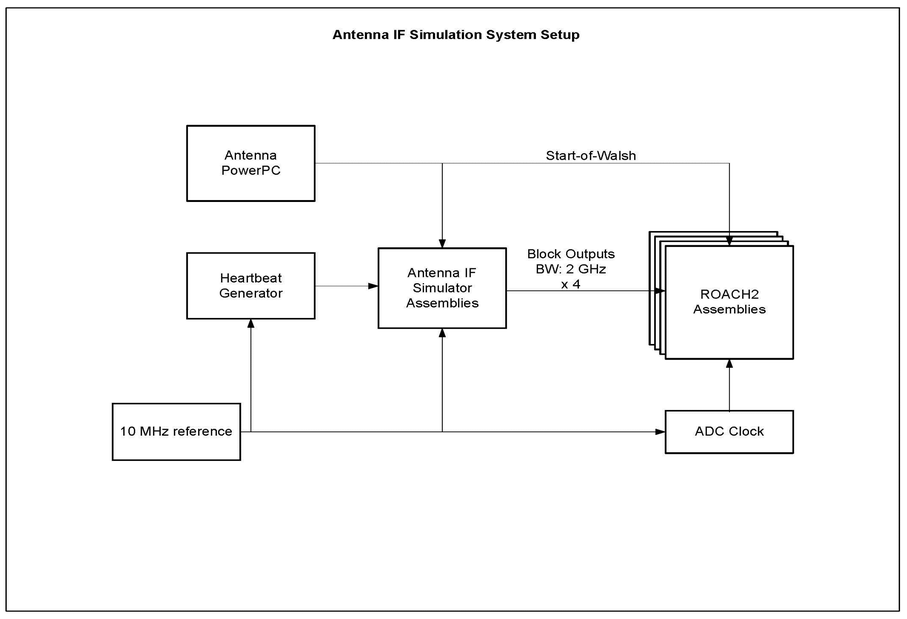
- 4 independent wideband correlated noise outputs with independent phase control.
- Walshing of the correlated noise outputs.
- Phase ramping of the correlated noise outputs.
- Synchronous phase switching of outputs on rising edge of 10 ms heartbeat signal.
- Processing of a start-of-Walsh signal.
- Option to sum uncorrelated noise with correlated noise outputs.
- Option to sum a tone with the correlated noise.
- Manual control of the amplitude of noise outputs using variable attenuators.
- Locked to common 10 MHz reference.
- Ethernet controllable

Hardware Design





System Setup



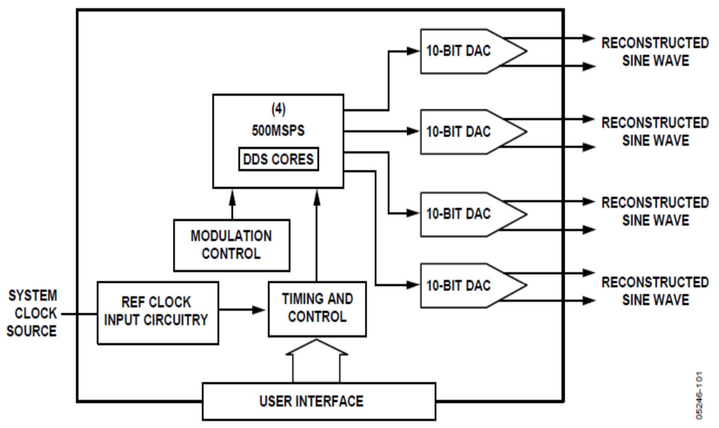
Hardware Control

A Digi-Com RCM4200 is the primary controller for the antenna simulator system.

- The processor module resides on a Digi-Com breadboard assembly.
- Start-of-Walsh and Heartbeat signals are level shifted and passed to the processors interrupt registers.
- On receipt of the Start-of-Walsh signal the heartbeat interrupt service register is enabled.
- On receipt of the rising edge of the heart beat signal the processor toggles the load phase register strobe on the AD9959 4 channel DDS evaluation board.
- It then computes the next set of phase values and loads the new phases into the AD9959's phase registers and waits for the next heartbeat.
- The AD9959 is programmed by passing register commands through an SPI interface. These commands are generated in the RCM4200 module using precompiled SPI libraries and are transmitted out of the one of the 4 available serial ports.

Controlling software is written in Dynamic C and compiled binaries are stored in the processors flash memory.

AD9959 Synthesizer



DDS synthesizer features

- 4 synchronized DDS channels @ 500 MSPS Independent frequency/phase/amplitude control between channels
- Matched latencies for frequency/phase/amplitude changes
- Excellent channel-to-channel isolation (>65 dB)
- 4 integrated 10-bit digital-to-analog converters (DACs) Individually programmable DAC full-scale currents
- 0.12 Hz or better frequency tuning resolution
- 14-bit phase offset resolution 10-bit output amplitude scaling resolution
- Serial I/O port interface (SPI) with enhanced data throughput

References: AD9959 block diagram and list of features taken from AD9959 data sheet; ©2005–2008 Analog Devices, Inc.