INCORPORATING PARTIAL RECONFIGURATION INTO THE CASPER TOOLFLOW

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As the size and complexity of FPGAs increase, so do compile times; the current CASPER tools recompile a design in its entirety for each call of the build process. Partial reconfiguration can be leveraged to exclusively compile the dynamic parts of the design. That is, those resources which change between modes of implementation for a given firmware base. In the case of CASPER, this allows the board support package of the target hardware to be precompiled and only the DSP be recompiled when generating a bitstream. This has the added benefit of reduced upload and configuration times due to smaller bitstream files and persistent communication interfaces, e.g. Ethernet, PCIe. SARAO is in the process of incorporating Partial Reconfiguration into the CASPER toolflow, with development targeted at the Ultrascale+ platforms including the VCU118 and VCU1525. This presentation aims to update the CASPER community on developments on this task and involve a wider audience in the discussion around its implementation.