ENABLING 100 GIGABIT ETHERNET ON THE VCU118/VCU1525 FOR CASPER

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The availability of 100G MAC on the Virtex UltraScale+ FPGAs has created a valuable resource for CASPER system designers to exploit. Work was done to enable the Xilinx 100G MAC core and interface it with AXI stream infrastructure on the rest of the CASPER VHDL firmware. A board support package to enable casper yellow blocks to connect to the 100G MAC is in development. In the work various architecture optimizations have been explored to enable non-blocking and high throughput interface to and from the 100G MAC.