MULTIBEAM DIGITAL BEAMFORMING ON 4-ELEMENT ARRAY AT 28 GHZ USING XILINX RF SOC ZCU1275

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The formation of simultaneous beams across a multitude of directions is an important aspect in many areas such as radio astronomy, imaging, phased-array radar and wireless communications. Multibeam beamforming is a key enabler for emerging millimeter wave (mmW) based 5th generation (5G) communication networks. Designers of 5G (and 6G) mmW wireless systems are considering digital implementations of multibeam beamformers, despite the high complexity, because of the advantages such as high flexibility and ability to utilize the full degrees of freedom from an array. Preliminary results of a 4-element 28 GHz digital array receiver, which is the first step towards a 28 GHz fully digital 16-element array receiver will be presented. The array receiver is implemented using commercial off-the-shelf electronics to support an 800 MHz channel bandwidth targeting mmW communication systems. A 28 GHz patch antenna sub-array that performs analog beamforming is designed to increase the gain in the elevation plane. The receivers are designed to work with orthogonal frequency division modulation (OFDM) supporting 3 Gbps data rate over the 800 MHz bandwidth and have been modeled in AWR Microwave Office using circuit models to design the optimum receiver electronics. A real-time digital signal processing (DSP) algorithm that generates 4-simultaneous beams operates on the Xilinx ZCU 1275 processing platform. The ZCU 1275 features the Xilinx Zynq UltraScale+ XCZU29DR Radio Frequency System on Chip (RFSoC). The XCZU29DR chip contains 16 12-bit ADCs (that supports sampling up to 2 GSPS) and 16 14-bit DACs (that supports sampling up to 6.4 GSPS). The details of the designed 28 GHz antenna will be presented along with the measured antenna responses. The architecture, design procedures and the electronics of the front-end receiver that can achieve 3 Gbps data rate over the 800 MHz bandwidth will be discussed. The ZCU 1275 board based digital back-end design specifics will be covered along with the architecture of the digital processing circuits and clocking mechanisms of the data converters. The initial results of the 4 simultaneous beam measurements will be presented.